The Beta-Multiplier: A Step-by-Step Guide to Understanding

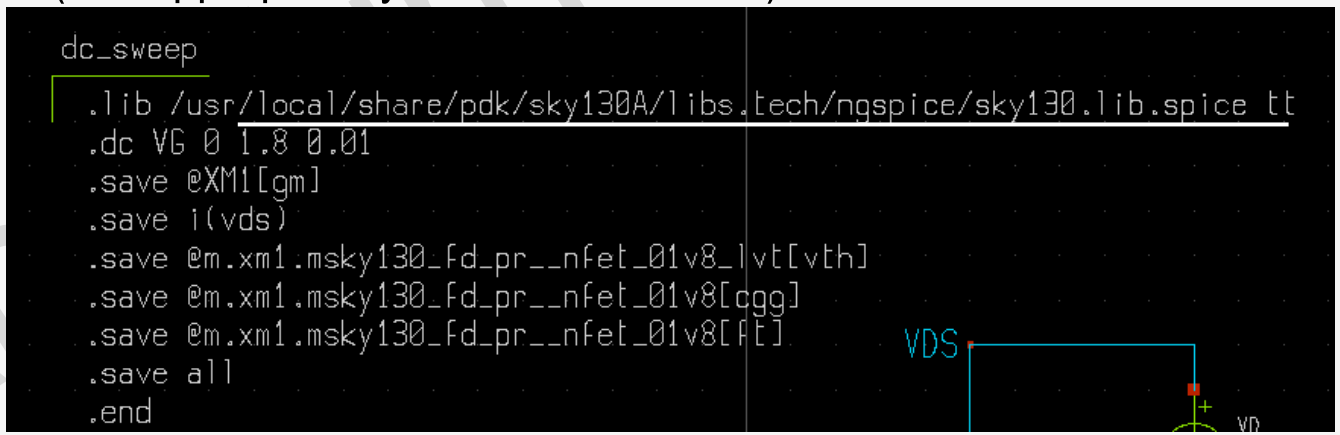
Dr. Anil Kumar Gundu

Important Points / Notes for the technology file incorporation SKY130A

- Pick the symbols either of the paths :
- /usr/local/share/pdk/sky130A/libs.tech/xschem/sky130_fd_pr/

  or
- /usr/local/share/pdk/sky130B/libs.tech/xschem/sky130_fd_pr/
- But make sure that library you are directing for the symbols you chose from above paths should be

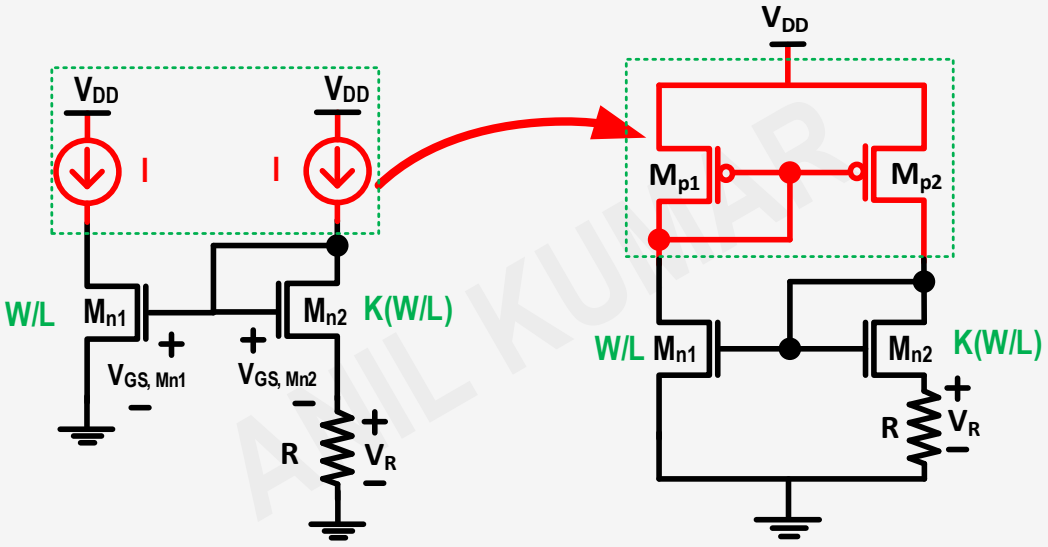
  .lib /usr/local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice tt
- tt means typical-typical corner (use appropriately the desired corner)



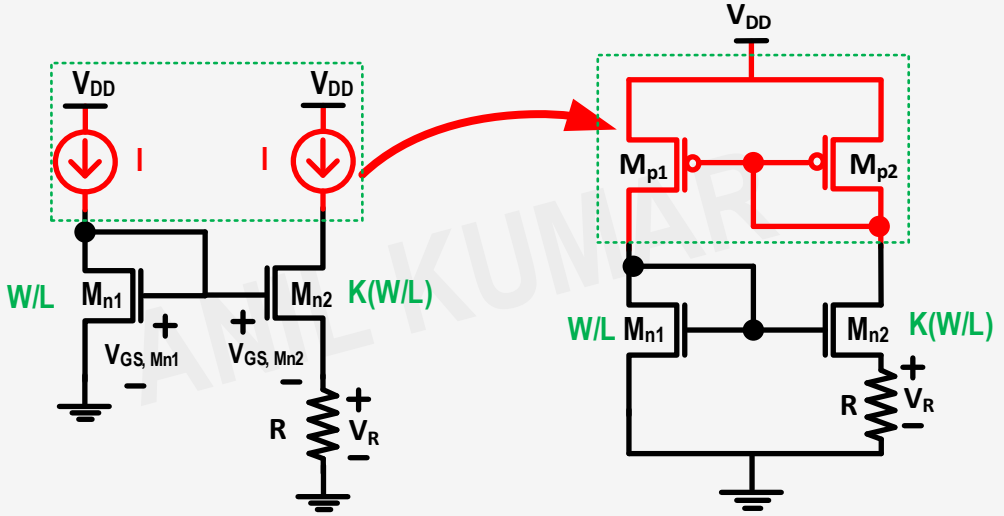
A Systematic and Simplified View of Beta-Multiplier

- One way to bias the devices M_{n1} and M_{n2} is to push the same current to both devices
- How can this be done? Use a matched current mirror (pmos in this case) as it will make sure that M_{n1} and M_{n2} carries same current
- We have two options to push same current to the devices M_{n1} and M_{n2} (shown below left and right):
  - Which option works without any problem

Option-1

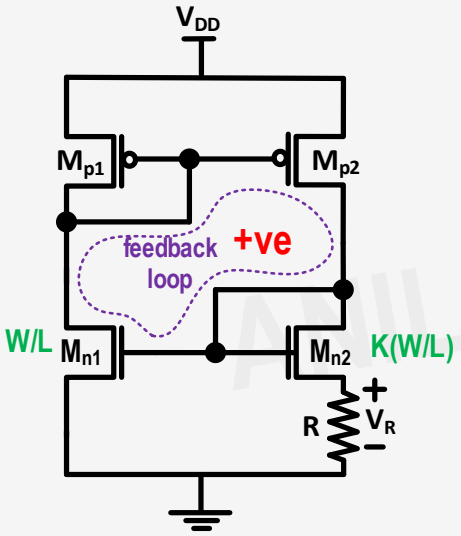


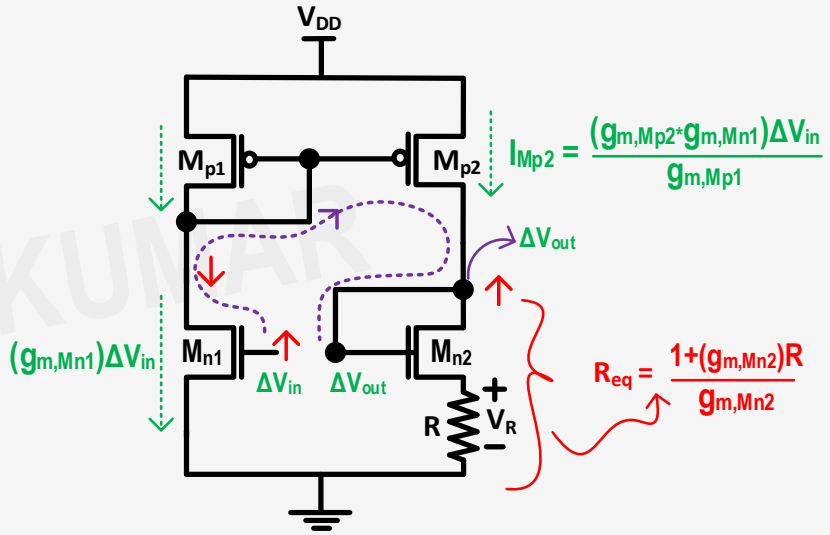
Option-2



A Systematic and Simplified View of Beta-Multiplier – Option 1

- It's a positive feedback loop. The loop gain is larger than 1.
- The loop gain and related analysis is shown below.
- The open loop gain in this case is strictly greater than 1 for any K > 1





$$\Delta V_{out} = \frac{1+(g_{m,Mn2})R}{g_{m,Mn2}} \frac{(g_{m,Mp2}*g_{m,Mn1})\Delta V_{in}}{g_{m,Mp1}}$$

$$g_{m,Mn2} = \sqrt{K}*g_{m,Mn1}$$

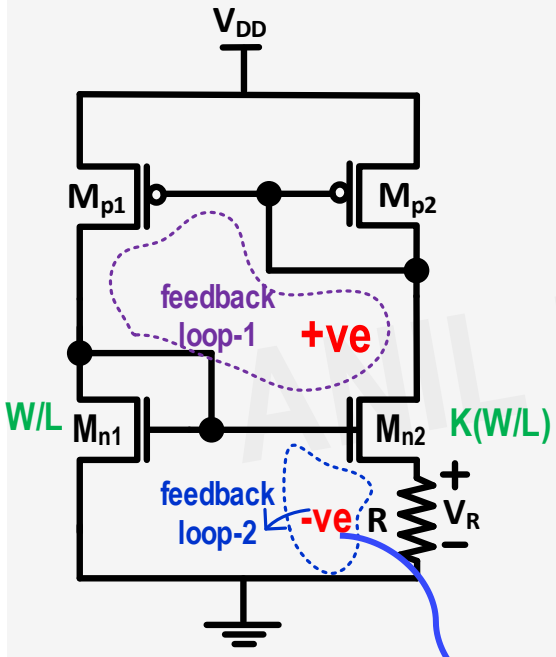
perfectly matched current mirror yield,

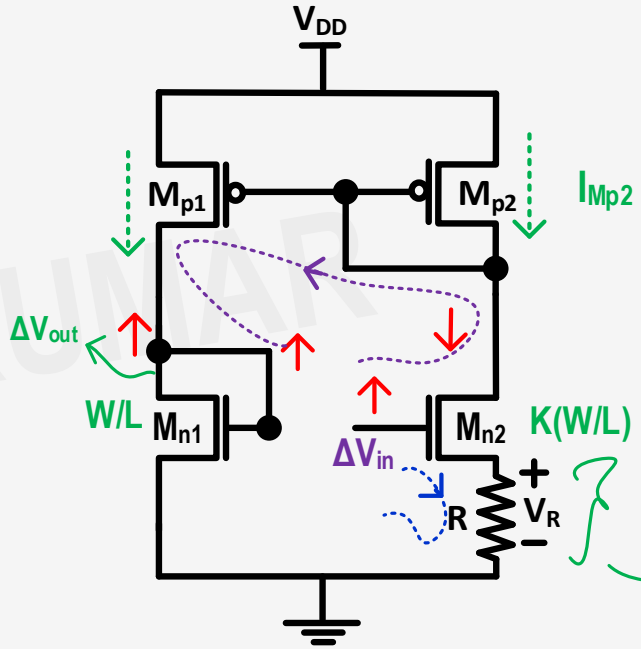
$$\Delta V_{out} = \frac{[1+(g_{m,Mn2})R](g_{m,Mn1})\Delta V_{in}}{g_{m,Mn2}}$$

$$\Delta V_{out} = \frac{[1+(g_{m,Mn2})R]\ \Delta V_{in}}{\sqrt{K}}$$

A Systematic and Simplified View of Beta-Multiplier – Option 2

- It's a positive feedback loop. But the loop gain is smaller than 1.
- The loop gain and related analysis is shown below.
- The open loop gain in this case is strictly less than 1 for any K > 1





$$I_{Mp2} = \frac{g_{m,Mn2}\Delta V_{in}}{(1+R*g_{m,Mn2})}$$

$$I_{Mp2} = V_R / R$$

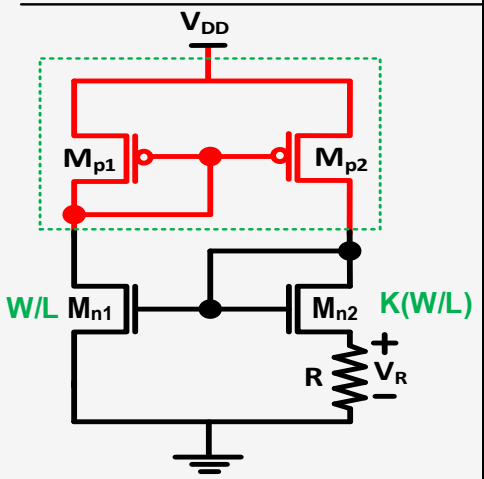
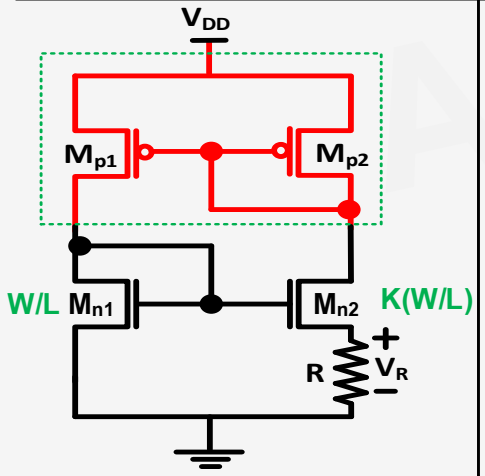
$$V_R = \frac{R*g_{m,Mn2}\Delta V_{in}}{(1+R*g_{m,Mn2})}$$

$$\Delta V_{out} = \frac{g_{m,Mn2}\Delta V_{in}}{(1+R*g_{m,Mn2})} \frac{1}{g_{m,Mn1}}$$

$$\Delta V_{out} = \frac{\sqrt{K}\Delta V_{in}}{(1+R*g_{m,Mn2})}$$

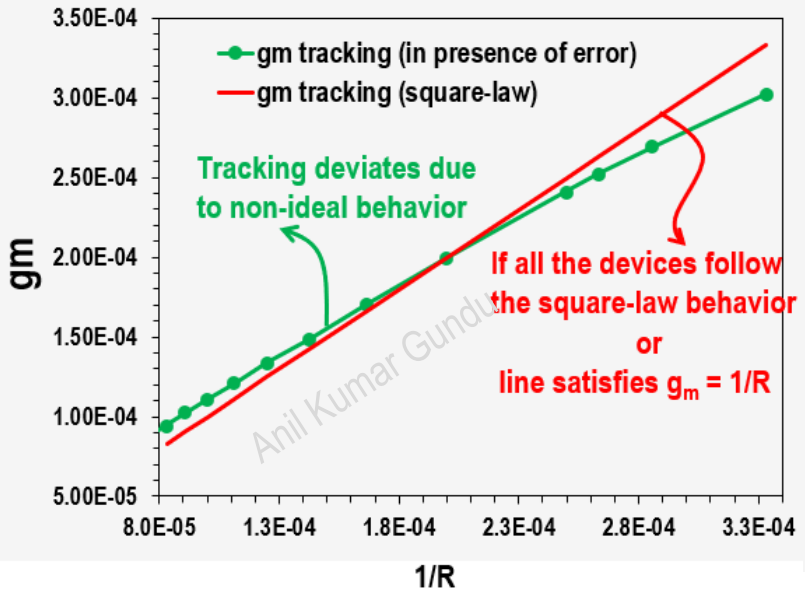
This loop effectively helps in keeping loop gain less than 1

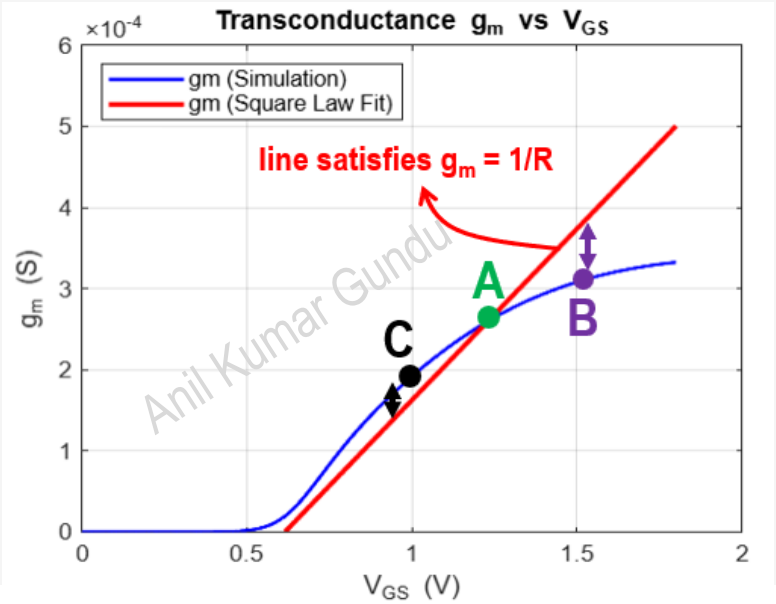
Beta-Multiplier at a Glance

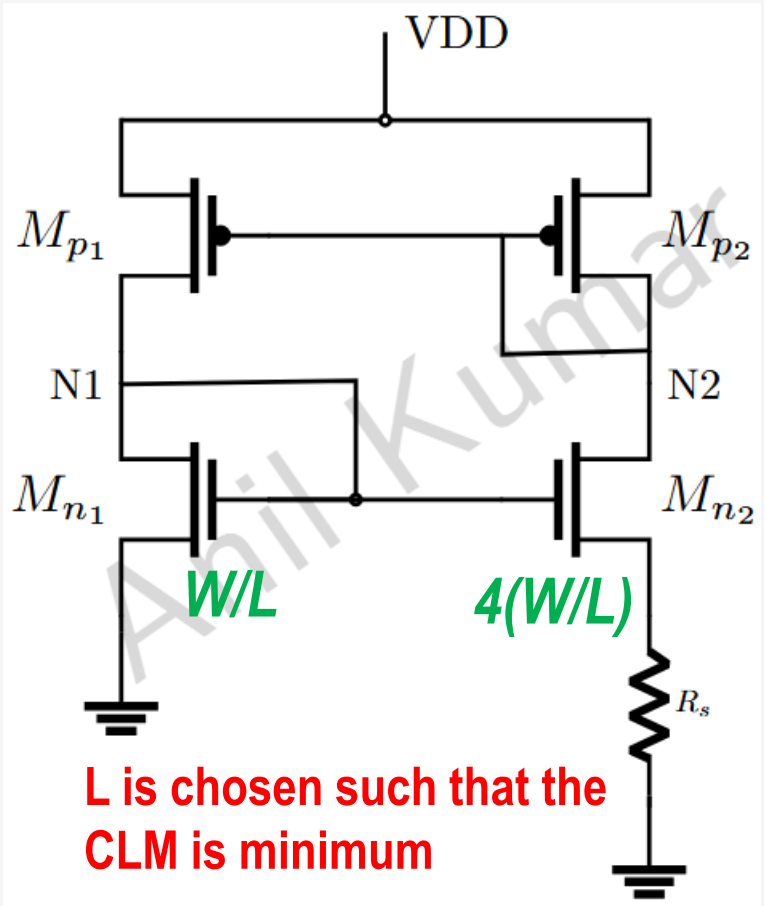
	feedback	DC Loop Gain	stability	gm
	positive	$\Delta V_{out} = \frac{2\sqrt{K}-1}{\sqrt{K}}\Delta V_{in}$ Loop gain is greater than 1 **> 1**	unstable	gm is not stabilized
	positive	$\Delta V_{out} = \frac{\sqrt{K}}{2\sqrt{K}-1}\Delta V_{in}$ Loop gain is less than 1 **< 1**	stable	$g_{m,Mn1}R = \frac{2(\sqrt{K}-1)}{\sqrt{K}}$ **(constant)**

Gm Tracking: Off-Chip Resistor Impact

- Let us say, for a given sizing of the devices, transconductance (gm) perfectly tracks the inverse of the off-chip resistor (R), meaning g_m=1/R and sets the operating point at ‘A’.
- Here's how variations in the resistor R affect the operating point and transconductance:
- If the resistor R increases to 2R:
  - Ideally, the current in device M_{n2} should halve and this current will be mirrored to M_{p1}
  - However, the operating point of M_{n1} shifts along the blue contour to 'C’.
  - This indicates that the actual gm is higher than its expected value (which should be 1/(2R)).
- Similarly, If the resistor R decreases to R/2. The operating point moves towards 'B’.
  - In this scenario, gm decreases, or. the devices may even **move out of saturation**



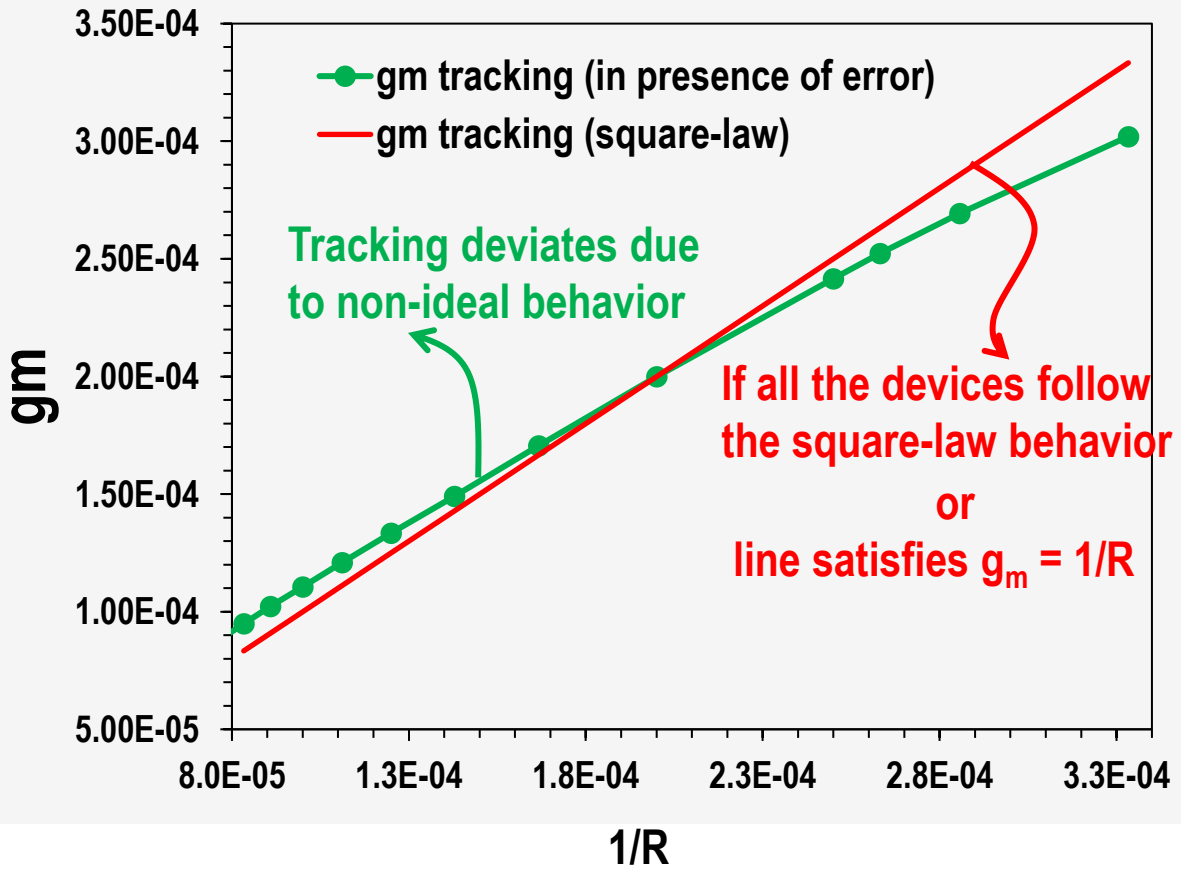


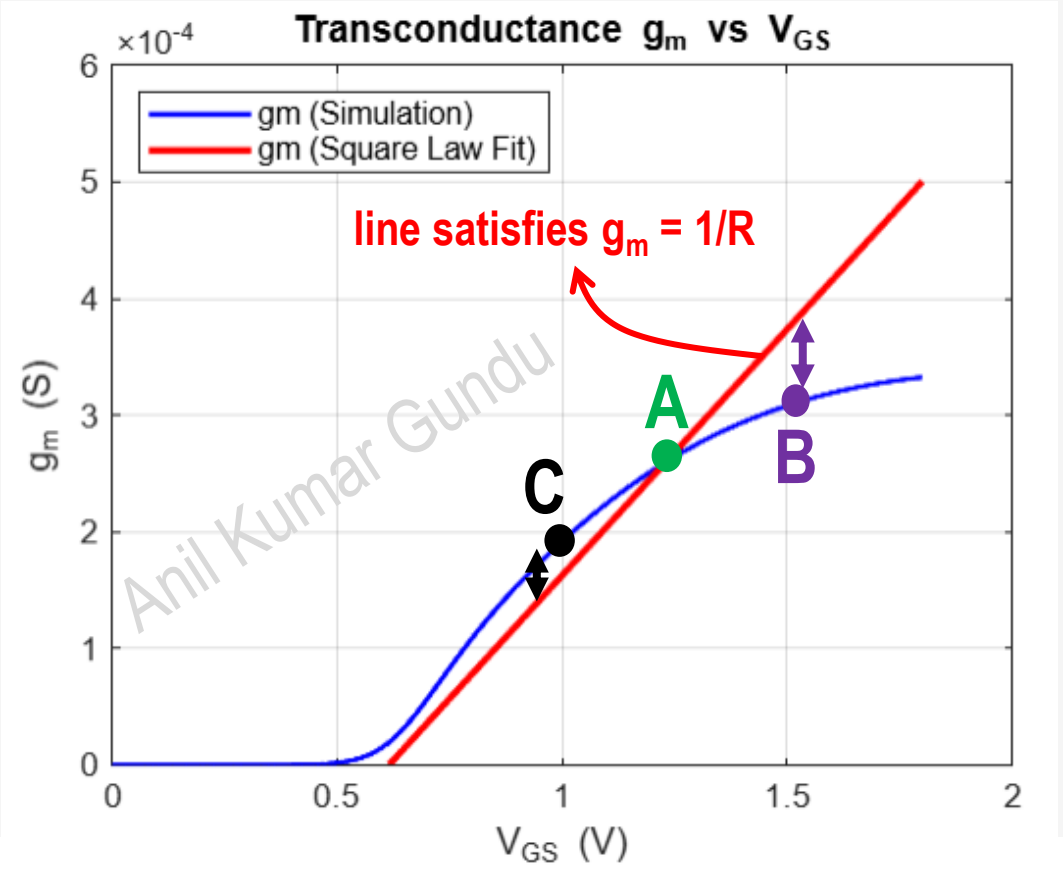


Characterized using opensource skywater 130nm PDK

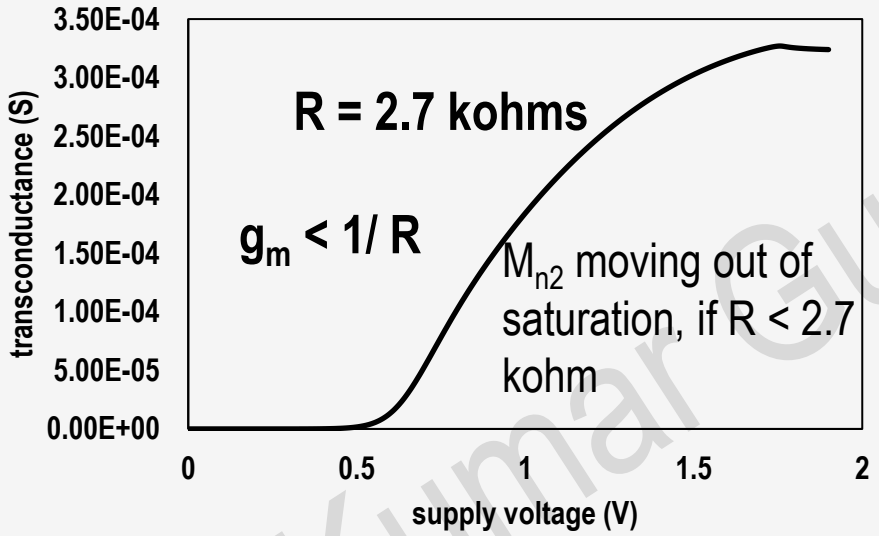
Gm Tracking: Off-Chip Resistor Impact

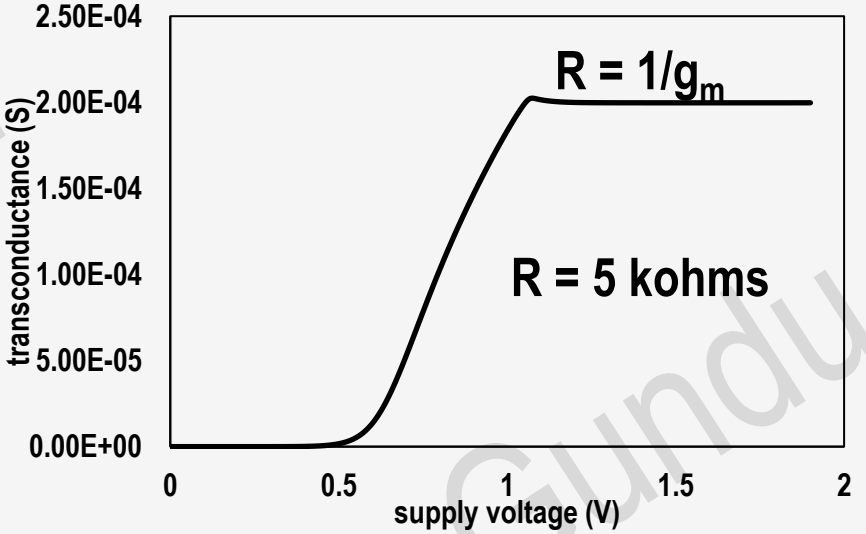
- If the off-chip resistor is increased or decreased, will this gm still be tracked accurately, if not how the error is going to behave.
- Let us say, for a given sizing of the devices, the gm is perfectly tracked and the gm = 1/R for the off-chip resistor of R. Now let's

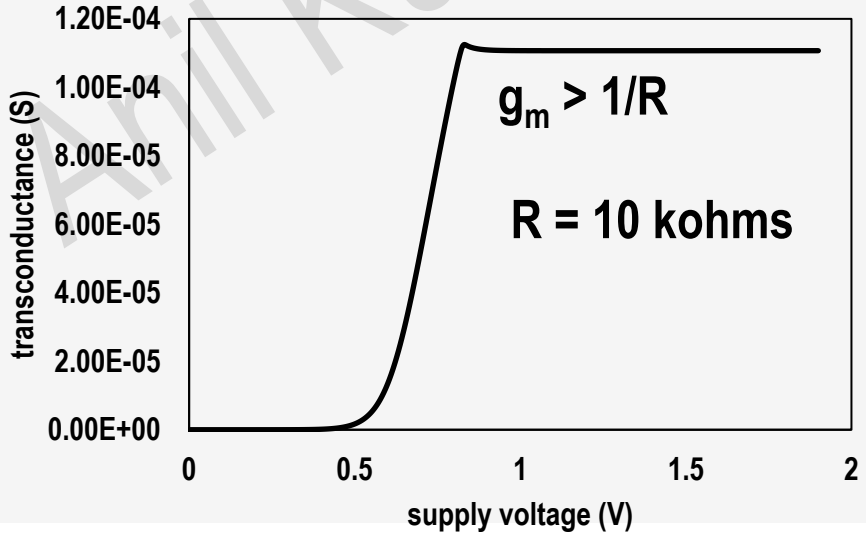


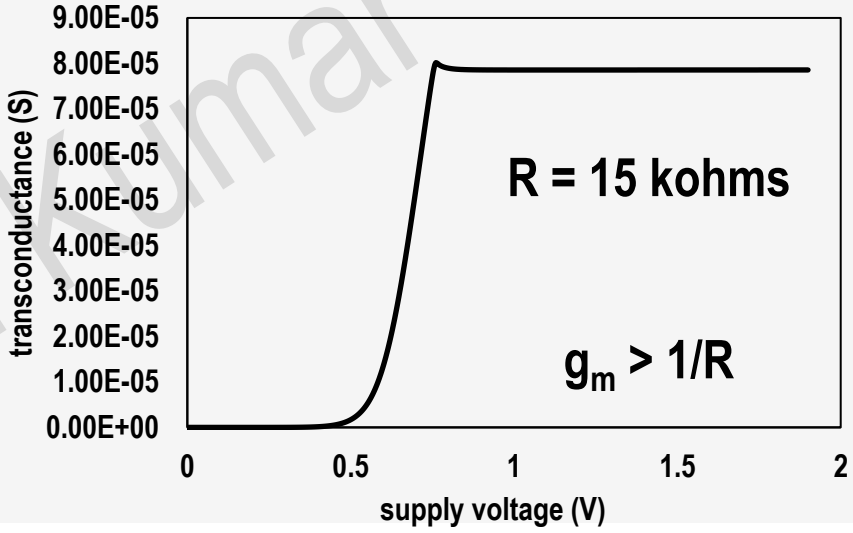


Simulations (SKYWATER 130nm PDK)

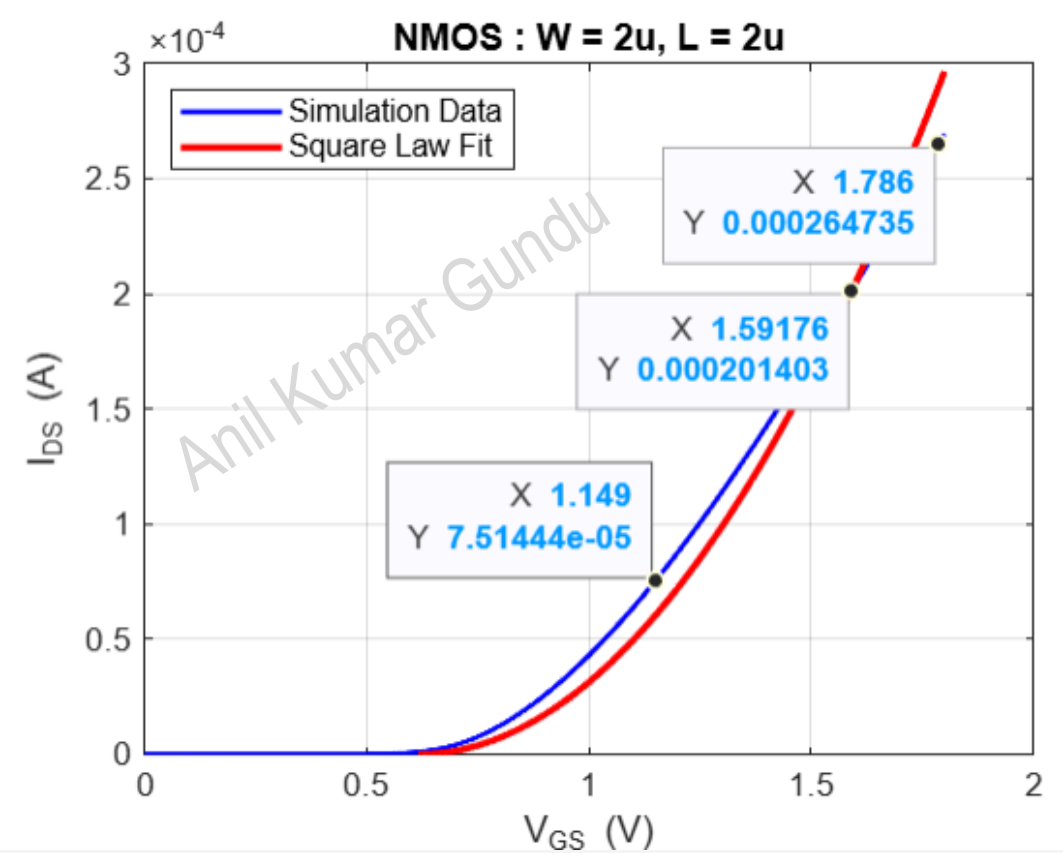


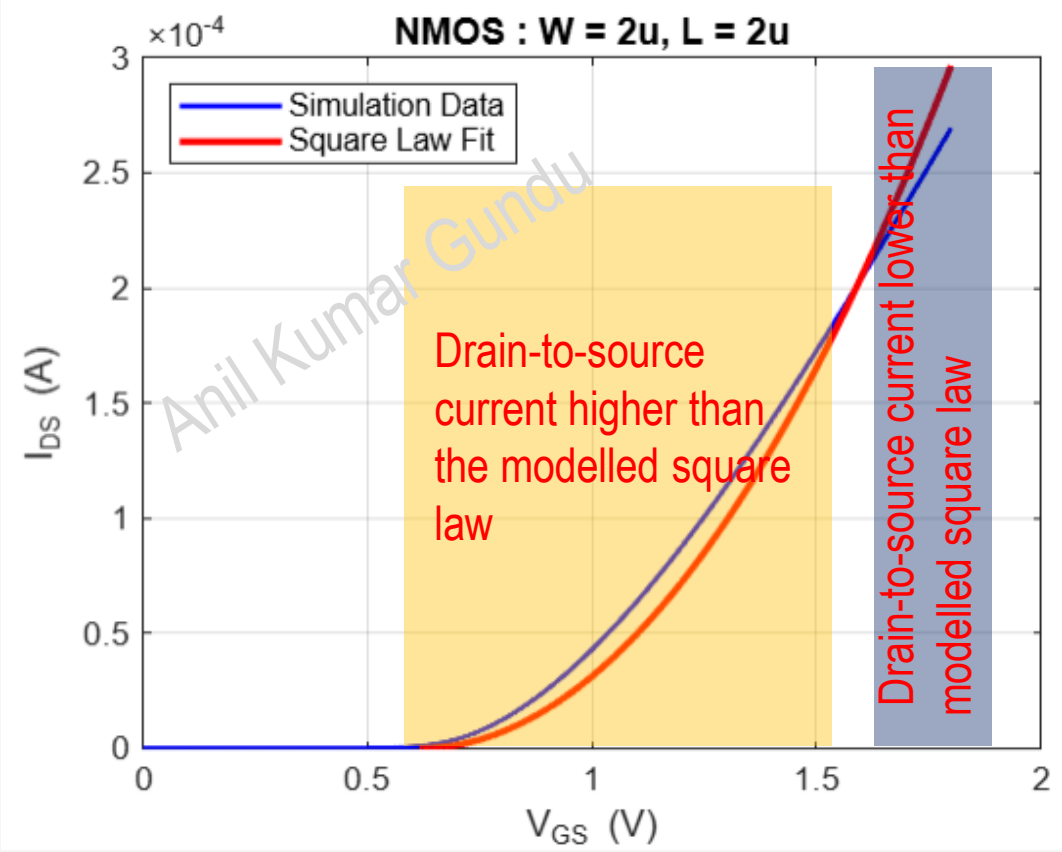






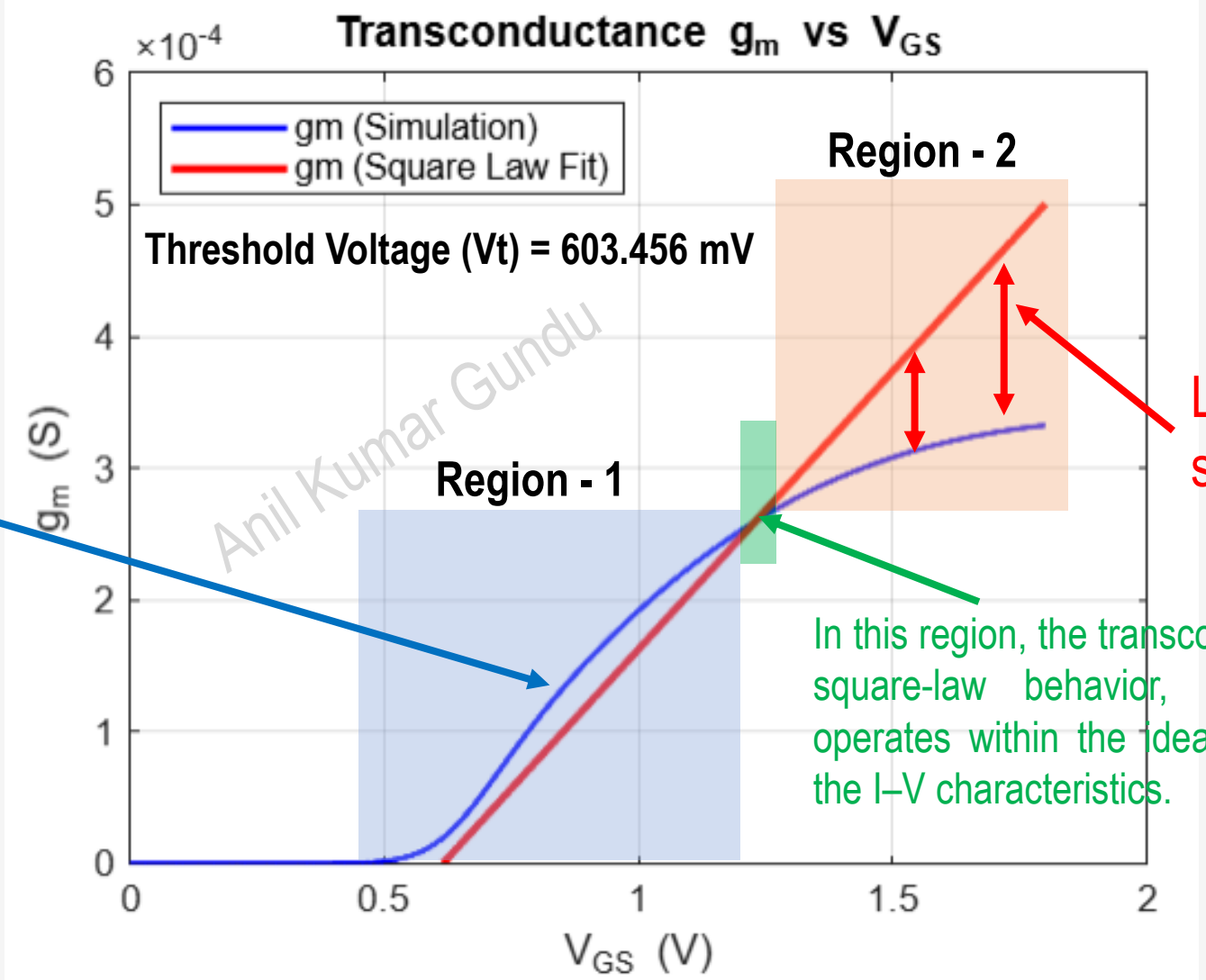
NMOS: W/L is (2um/1um) and VDS is 1.8V and VGS is varied from 0V to 1.8V





Threshold Voltage (Vt) = 603.456 mV

NMOS: W/L is (2um/1um): Transconductance plot and square law fit



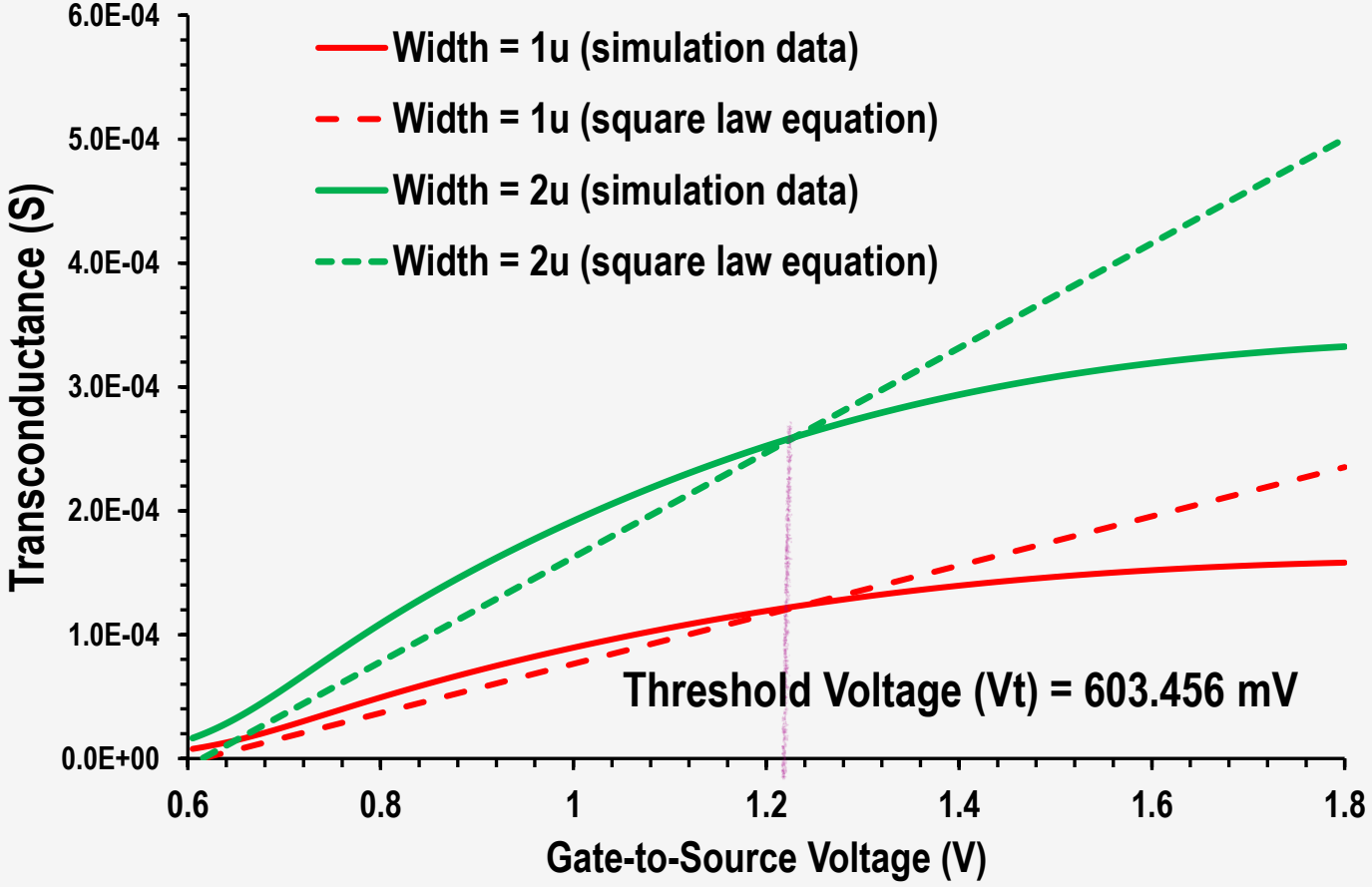
Little deviation from square law model

Larger deviation from square law model

In this region, the transconductance matches the square-law behavior, indicating the device operates within the ideal square-law regime of the I–V characteristics.

NMOS Transconductance Characterization (V_{DS} is 1.8V and V_{GS} is varied from 0V to 1.8V)

- *When varying the current in a MOS device of a given size (from maximum to minimum or vice versa), the transconductance aligns with the ideal square law at a particular current value. The further the current moves from this point, the greater the error or deviation*



- We often approximate the I_{DS}–V_{GS} relationship with a square law, but in reality, the current scales with V_{GS} to an exponent typically ranging from 1 to 2. This non-ideal behavior means that relying on the simple square law equation will result in significant deviation in the calculated transconductance g_m.

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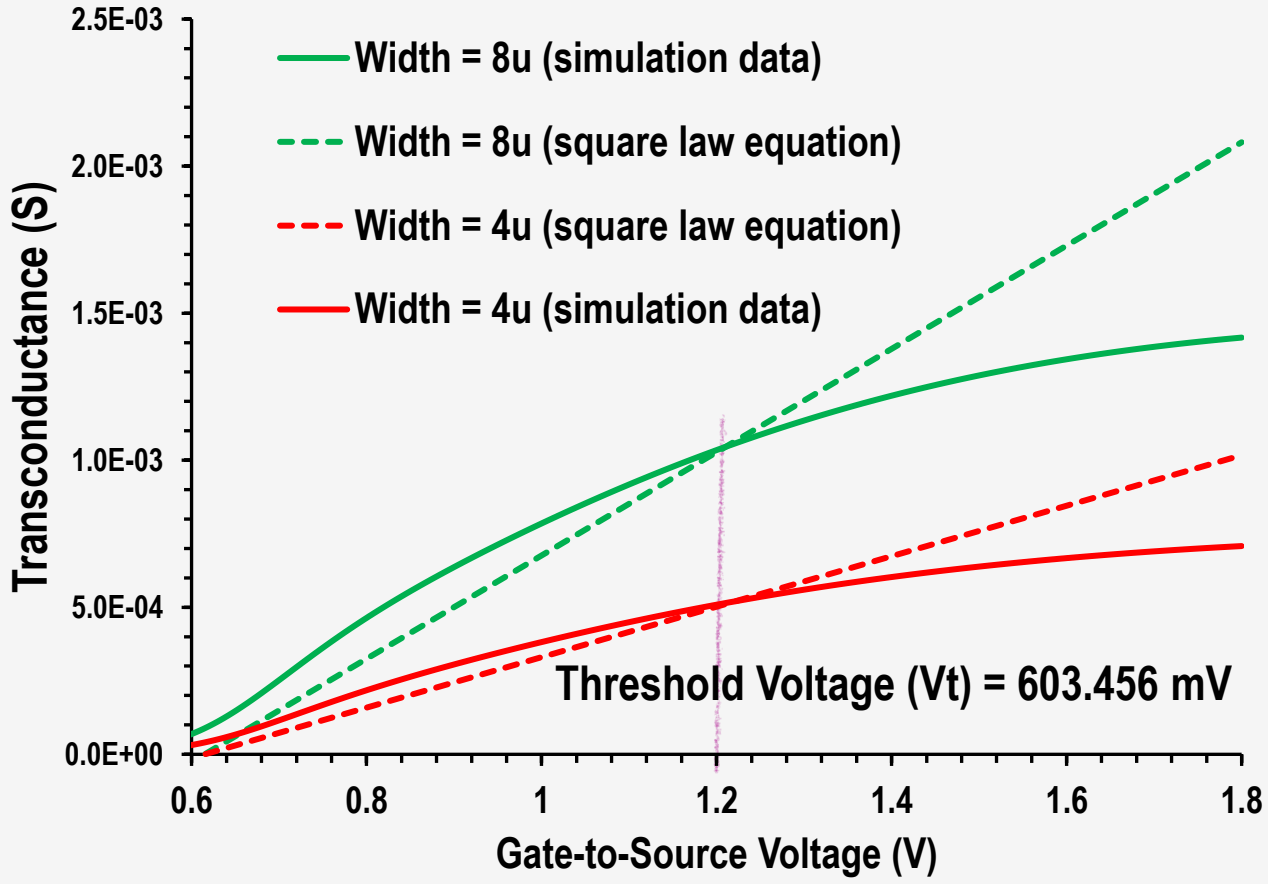

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Appendix

PMOS Critical Data : Threshold Voltage

- Threshold voltage of the nmos (130nm google SKY130A) devices are extracted at a nominal temperature of 27°C for the following devices (TT corner):
- Width = 1um and L = 0.15um

Device	Device	VDD (max)	Type	Threshold Voltage (mV)
pfet_01v8	PMOS	1.8	Nominal	510.3
pfet_01v8_hvt	PMOS	1.8	High V_t	660.9
pfet_01v8_lvt	PMOS	1.8	Low V_t	282.5
pfet_01v8_nf	PMOS	1.8	Nominal V_t (with fingers)	510.3
pfet_01v8_hvt_nf	PMOS	1.8	High V_t (L =0.35u with fingers)	775.6
pfet_01v8_lvt_nf	PMOS	1.8	Low V_t (with fingers)	282.5

- More details on the device voltages and their characteristics, refer

https://skywater-pdk.readthedocs.io/en/main/rules/device-details.html

NMOS Critical Data: Threshold Voltage

- Threshold voltage of the nmos (130nm google SKY130A pdk) devices are extracted at a nominal temperature of 27°C for the following devices (TT corner):
- Width = 1um and L = 0.15um

Device	Device	VDD (max)	Type	Threshold Voltage (mV)
nfet_01v8	NMOS	1.8	Nominal	769.2
nfet_03v3_nvt	NMOS	1.8	Native V_t	0
nfet_01v8_lvt	NMOS	1.8	Low V_t	570.48
nfet_01v8_nf	NMOS	1.8	Nominal V_t (with fingers)	769.2
nfet_01v8_esd_nvt_nf	NMOS	1.8	Native V_t (with fingers)	686.5
nfet_01v8_lvt_nf	NMOS	1.8	Low V_t (with fingers)	570.48
Nfet_20v0_nf	NMOS	20	Zero V_t	0

- More details on the device voltages and their characteristics, refer

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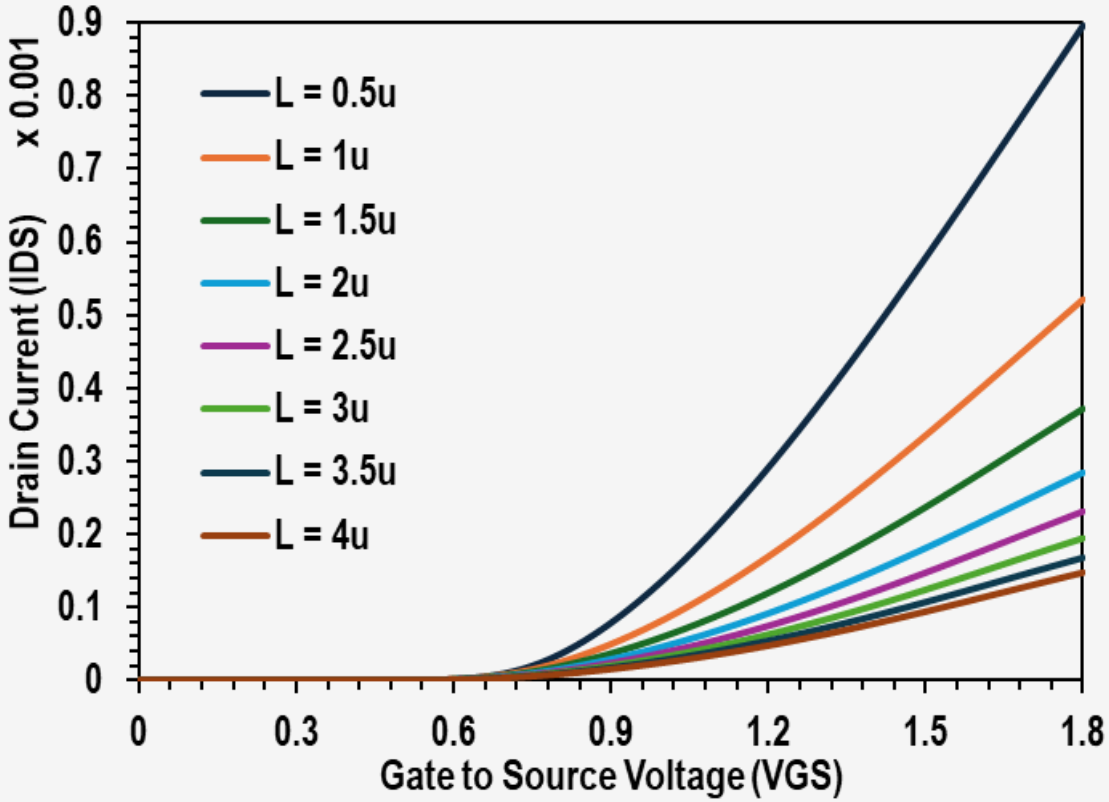
NMOS: Square Law Fitting (Ids vs Vgs)

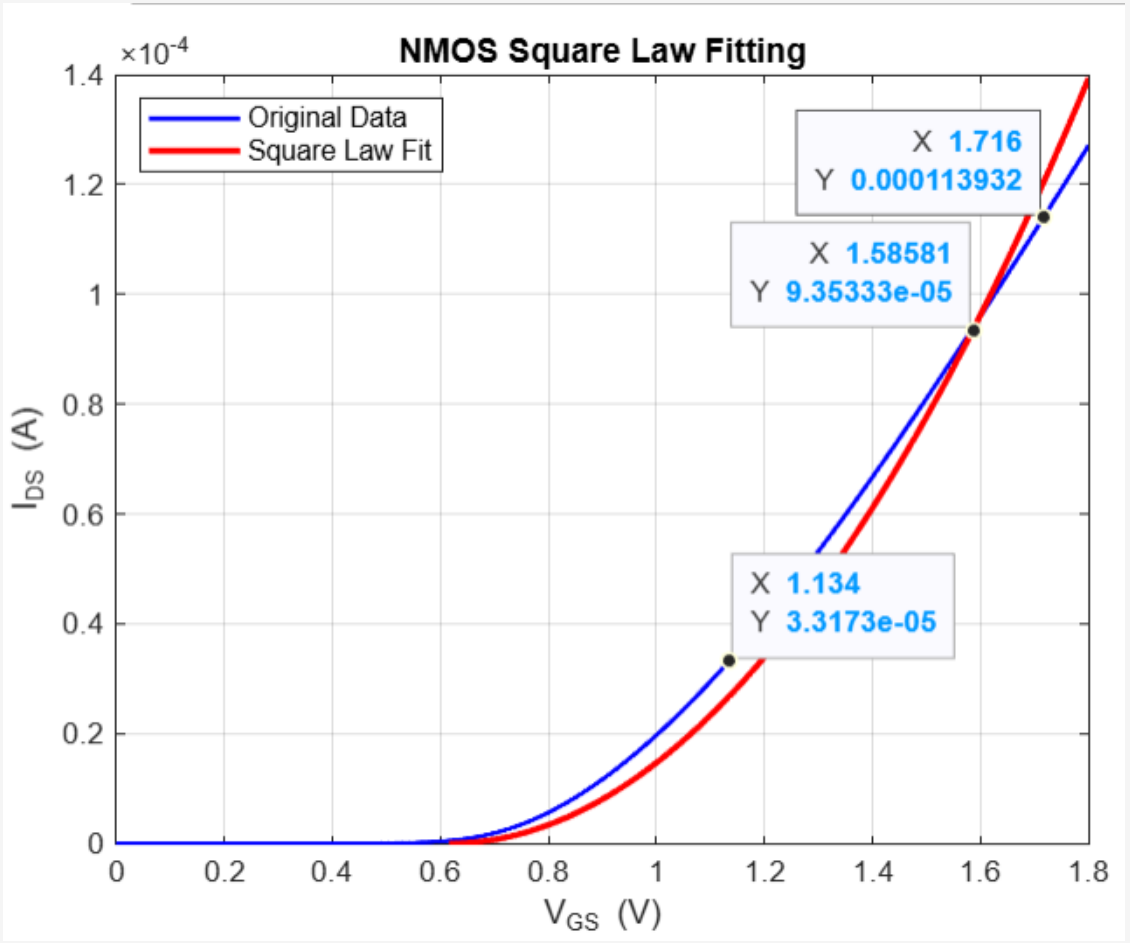
- Channel length of the NMOS is varied for an NMOS with width of 4um and then the square law equation is fitted.
- Approximately the Vth is chosen (approximately chosen) and checked the R^2 value.
- Device is forming mostly square law

Length (µm)	K	R^2
0.5	0.000537	0.9967
1	0.000307	0.9975
1.5	0.000217	0.9983
2	0.000165	0.9985
2.5	0.000134	0.9986
3	0.000113	0.9986
3.5	9.71e-05	0.9986
4	8.53e-05	0.9987



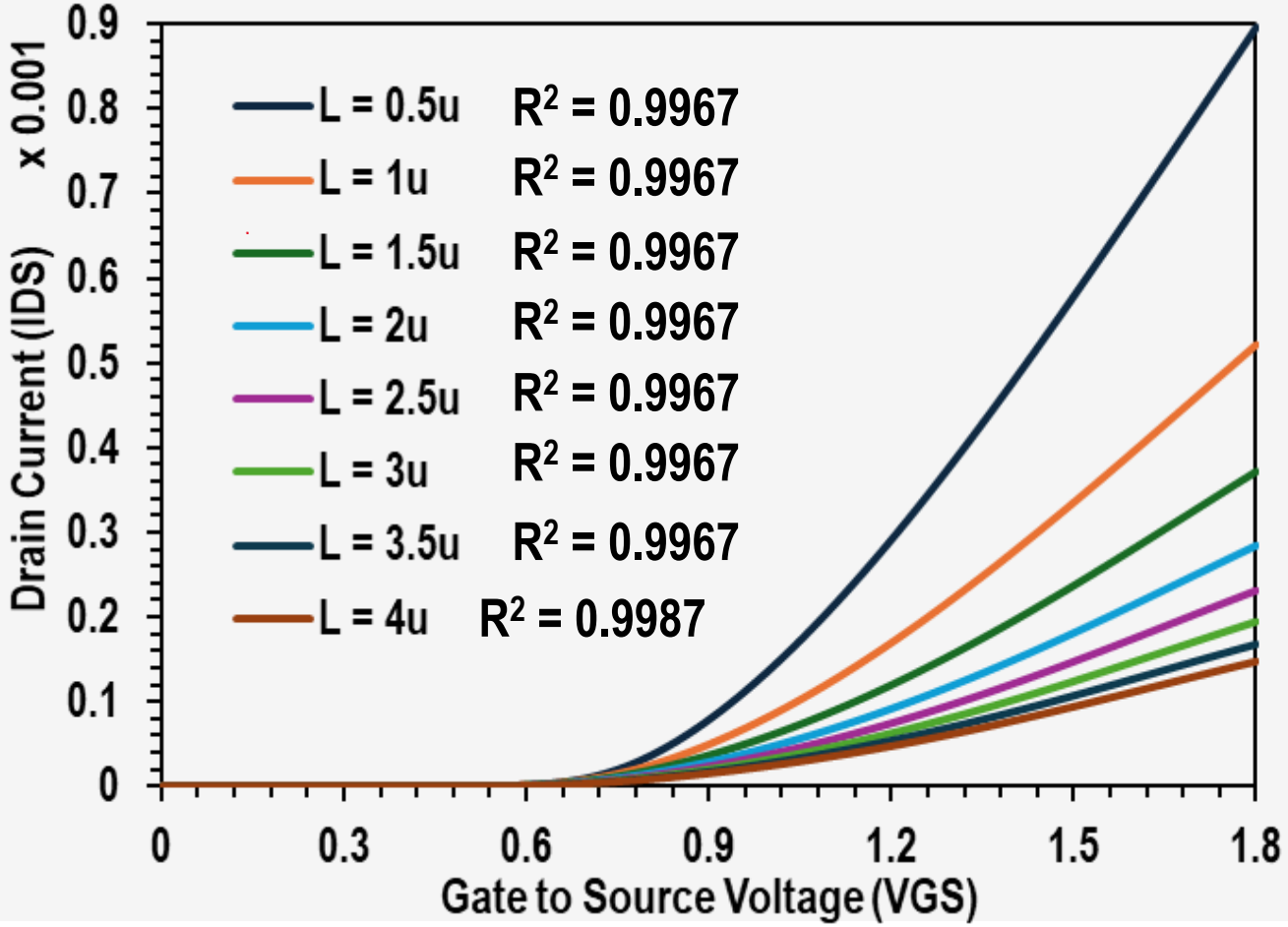
NMOS: W/L is (1um/1um) and VDS is 1.8V and VGS is varied from 0V to 1.8V

- Define an Operating Point: First, establish a specific operating point for the MOSFET by determining values for gate-to-source voltage (V_{GS}), drain current (I_{DS}), and drain-to-source voltage (V_{DS}).
- Differentiate I_{DS} with respect to V_{GS} : The transconductance (gm) is fundamentally the rate of change of the drain current (I_{DS}) concerning the gate-to-source voltage (V_{GS}) around the chosen operating point. Mathematically, it's expressed as g m = $\partial V_{GS}/\partial I_{DS}$.
- Utilize Square-Law Approximation for Analysis: To gain insight into gm , you can fit the measured or simulated I_{DS} vs. V_{GS} data to a square-law equation. This comparison helps to assess whether the actual I_{DS} is changing more slowly or quickly than predicted by the ideal square-law model, indicating if g m is underestimated or overestimated.



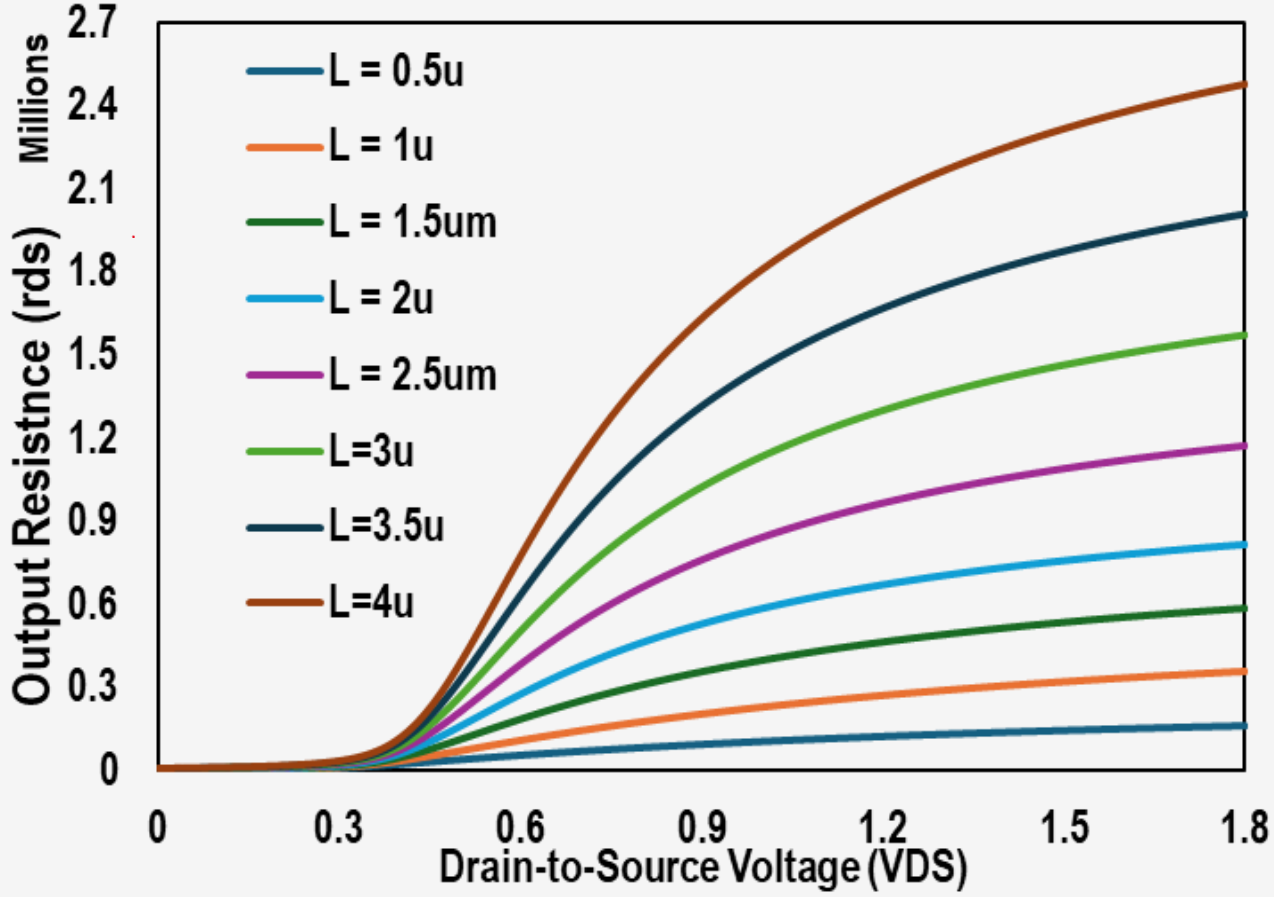
NMOS: Square Law Fitting (Ids vs Vgs)

- Channel length of the NMOS is varied for an NMOS with width of 4um and then the square law equation is fitted.
- Approximately the Vth is chosen (approximately chosen) and checked the R^2 value.

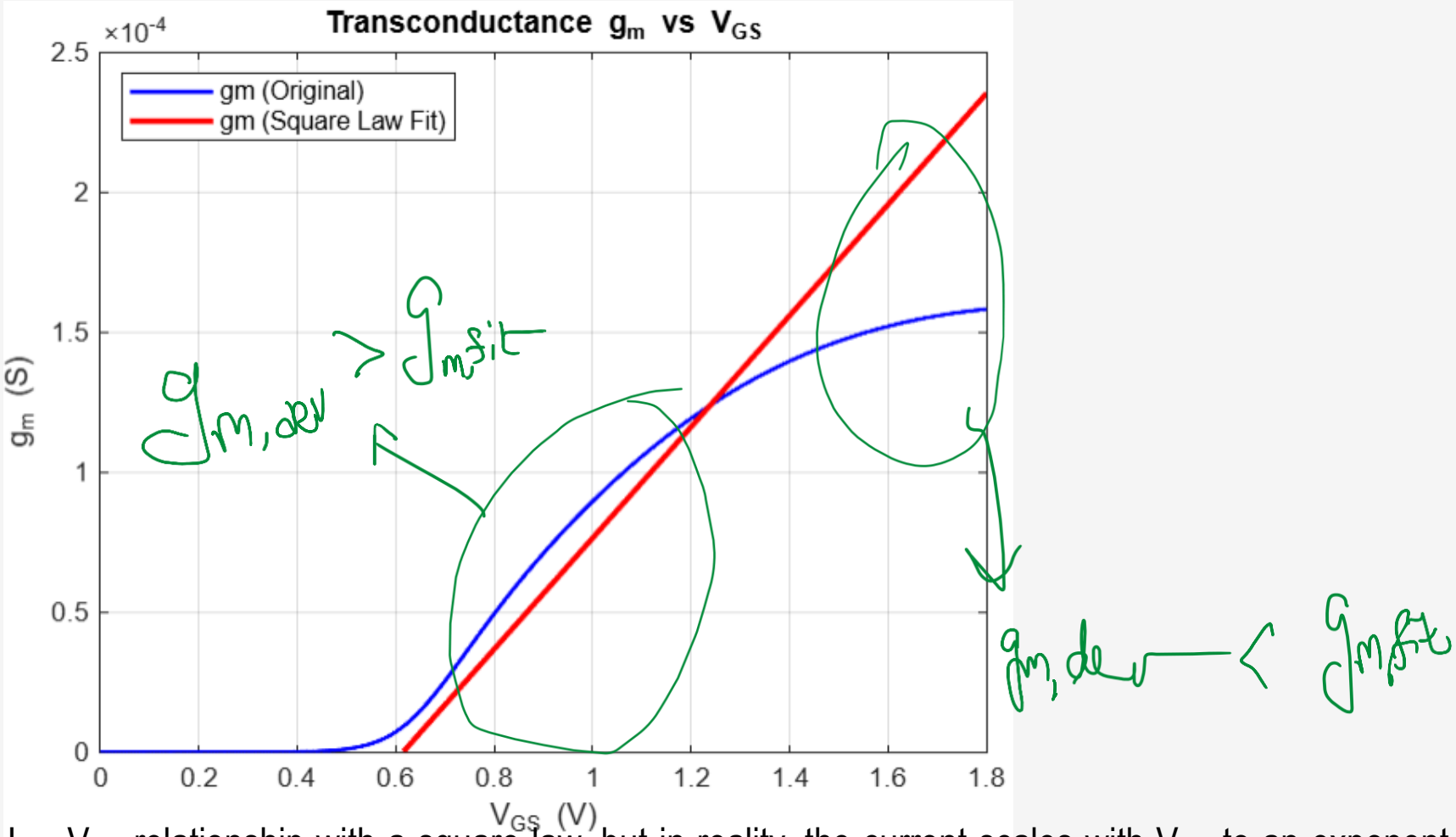


NMOS: Drain-to-Source Resistance

- Channel length of the NMOS is varied for an NMOS with width of 4um.
- Rds is plotted for various channel lengths.



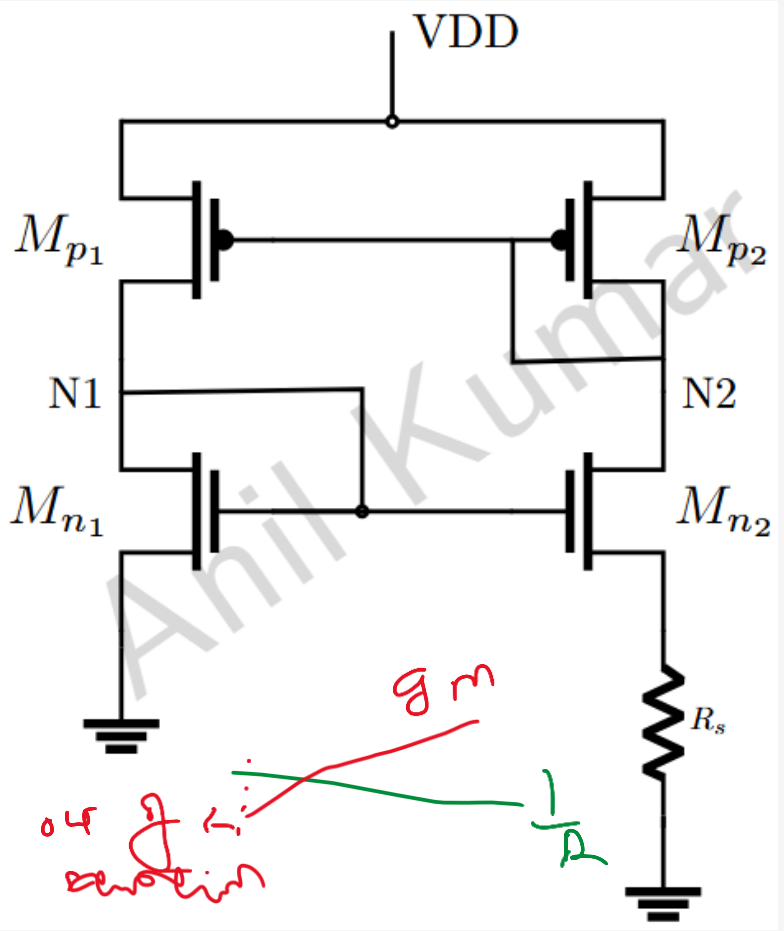
NMOS: W/L is (1um/1um) and VDS is 1.8V and VGS is varied from 0V to 1.8V



- We often approximate the I_{DS}–V_{GS} relationship with a square law, but in reality, the current scales with V_{GS} to an exponent typically ranging from 1 to 2. This non-ideal behavior means that relying on the simple square law equation will result in significant deviation in the calculated transconductance g_m.

Gm tracking with off-chip resistor and error understanding

- This circuit ensures that the transconductance (gm) of transistor Mn1 closely tracks the inverse of the off-chip resistor value (i.e., $gm_{mn1} \approx 1/R$), provided that the width-to-length (W/L) ratio of Mn2 is scaled to be four times that of Mn1 (i.e., $(W/L)_{mn2} = 4 \times (W/L)_{mn1}$).
- Assuming the off-chip resistance varies within a range from R_{min} to R_{max}, with a value R (where square-law equation holds), we analyze the impact on tracking accuracy. As the resistance R increases, the expected transconductance (1/R) decreases.
- However, due to nonidealities such as channel-length modulation, mismatch, and limited loop gain, the tracked gm_{mn1} tends to overshoot, resulting in $gm_{mn1} > 1/R$.
- Conversely, when the off-chip resistance R decreases, the circuit attempts to track a higher target transconductance. In this case, the limitations in biasing and device operation may cause gm_{mn1} to undershoot the ideal value, resulting in $gm_{mn1} < 1/R$.



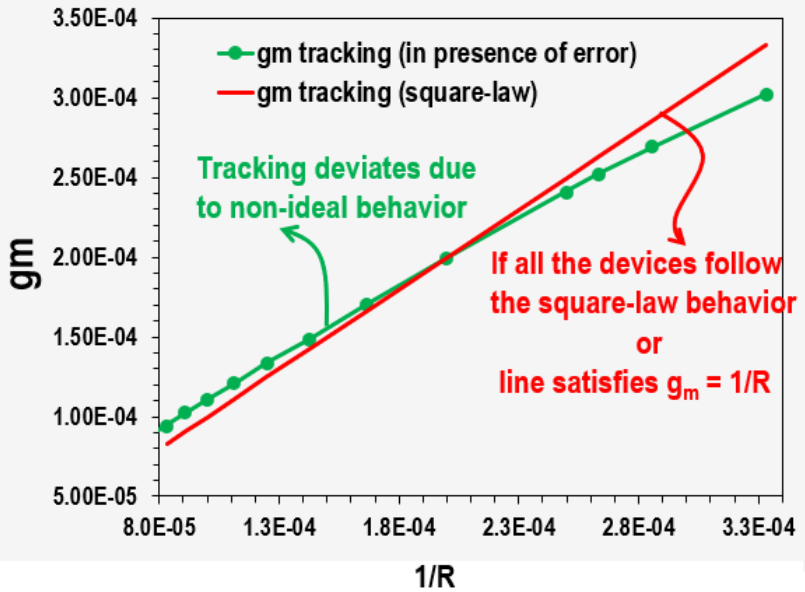
- This deviation from ideal tracking becomes more significant toward the extremes of the resistor range and should be carefully considered in the design and calibration of gm-based analog blocks.

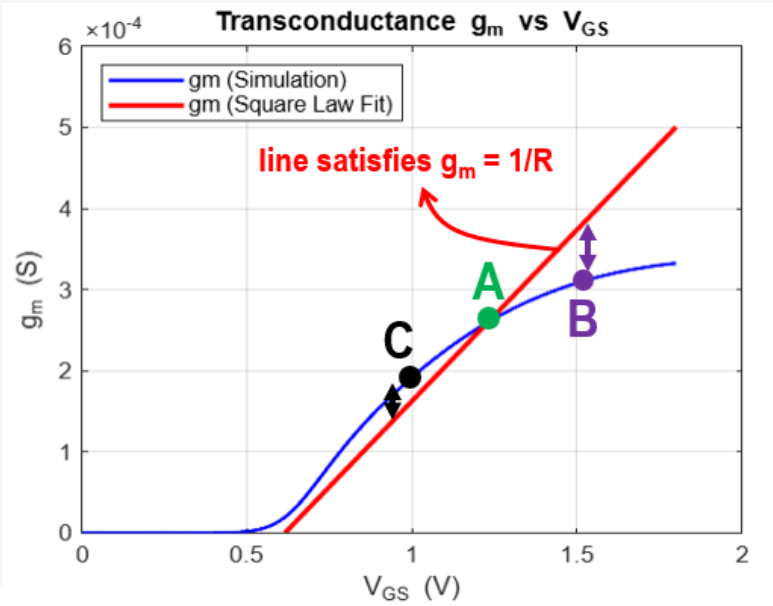
Gm tracking with off-chip resistor and error understanding

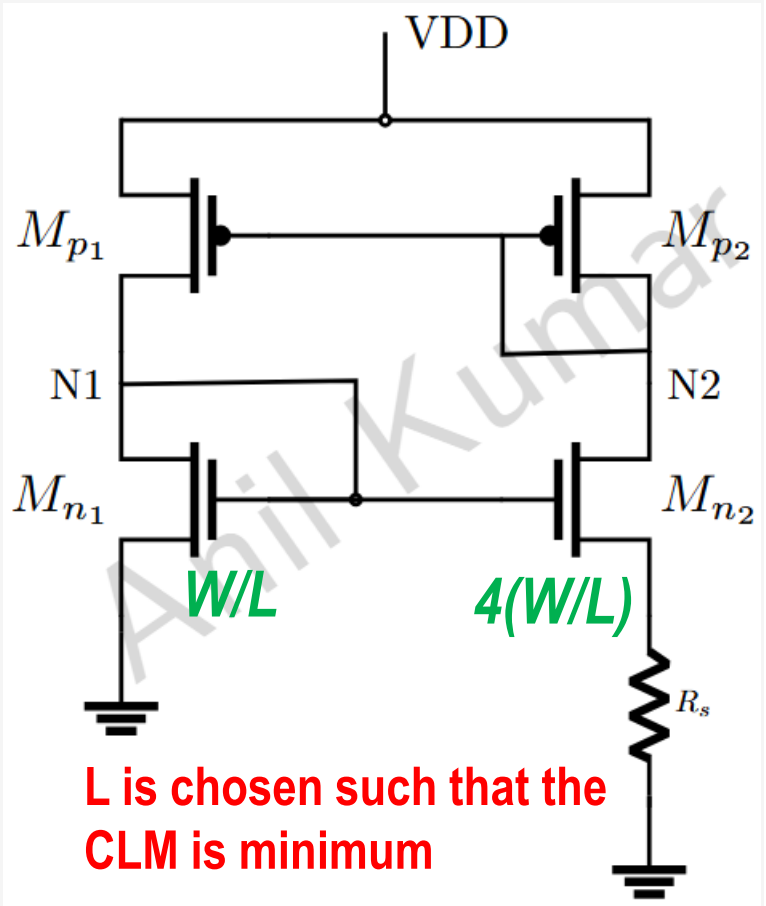
- While the beta-multiplier is designed to precisely control the transconductance (g_m) of a MOSFET (or one of the application) using an off-chip resistor, it is important to understand how precisely the transconductance of the device can be tracked with off-chip resistor.
- It's important to recognize that typical design analyses often assume the validity of the square-law equation for MOSFETs. However, this assumption does not hold true, even for devices with long channel length, due to various non-ideal effects.
- Hence it is very important to characterize and, at a minimum, qualitatively determine whether variations in the off-chip resistor lead to an underestimation or overestimation of the MOSFET's transconductance.

Gm tracking with off-chip resistor and error understanding

- Let us say, for a given sizing of the devices, transconductance (gm) perfectly tracks the inverse of the off-chip resistor (R), meaning g_m=1/R and sets the operating point at ‘A’.
- Here's how variations in the resistor R affect the operating point and transconductance:
- If the resistor R increases to 2R:
  - Ideally, the current in device M_{n2} should halve and this current will be mirrored to M_{p1}
  - However, the operating point of M_{n1} shifts along the blue contour to 'C’.
  - This indicates that the actual gm is higher than its expected value (which should be 1/(2R)).
- Similarly, If the resistor R decreases to R/2. The operating point moves towards 'B’.
  - In this scenario, gm decreases, or. the devices may even **move out of saturation**



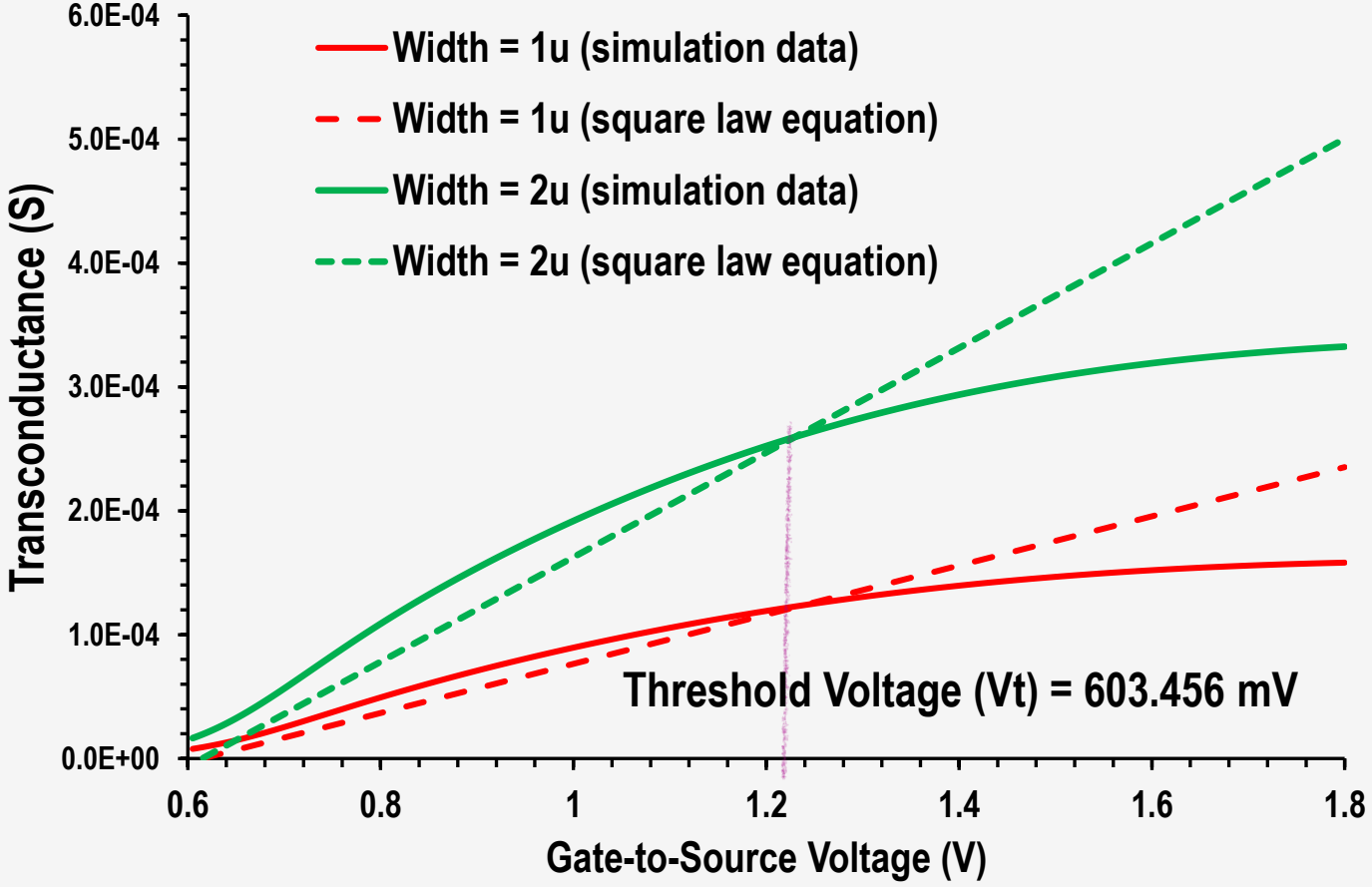




Characterized using opensource skywater 130nm PDK

Ideas to develop

- Finding the intersection point of both gm's after fitting the nearest square-law equation.
- If the device is biased to this current, it will hold all the square-law equations.
- Next step …. Next step …. (think)
- In this way, we can design the beta multiplier that exactly matches to off-chip resistor value



- We often approximate the I_{DS}–V_{GS} relationship with a square law, but in reality, the current scales with V_{GS} to an exponent typically ranging from 1 to 2. This non-ideal behavior means that relying on the simple square law equation will result in significant deviation in the calculated transconductance g_m.

Sizing of the Beta - Multiplier

- V_{DD} = 1.8V. Choosing the appropriate PMOS and NMOS devices to allow better overdrive. In the SKY130A pdk, very little options of NMOS and PMOS devices are available.
- The lowest Vt of NMOS device apart from native and zero Vt is LVT device which is as high
- PMOS has nominal transistor flavor with ~510mV and LVT flavor with as low as ~280mV
- Let's choose NMOS with LVT and PMOS with LVT flavors for the beta multiplier design

Device	Device	VDD (max)	Type	Threshold Voltage (mV)	V_{SG} (V)	V_{SD} (V)
nfet_01v8_lvt_nf	NMOS	1.8	Low V_t (with fingers)	570.48	1	1.8
pfet_01v8_lvt_nf	PMOS	1.8	Low V_t	282.5	1	1.8