Anil Kumar Gundu

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RESEARCH INTEREST

My research interests lie in developing circuits and systems that seamlessly integrate the physical world with digital information, particularly through self-powered systems (energy harvesting) and battery-indifferent circuit design.

EXPERIENCE

National University of Singapore **June 2022 - Present**
Post-doctoral Researcher
Green IC Lab
SHINE Centre - Singapore

Nanosystem Fabrication Facility (NFF) **August 2018 - January 2020**
User and Member
Clean Room 100/1000
HKUST, Hong Kong

IIIT - Delhi, New Delhi **July 2015 - January 2017**
Teaching Fellow

ST Microelectronics, Greater Noida **June 2014 - June 2015**
Trainee

EDUCATION

The Hong Kong University of Science and Technology **February 2017 - December 2021**
Doctor of Philosophy

Advisor: Prof. Volkan Kursun
Thesis: Static Random-Access Memory Circuits with 3D Stacked Nanosheet Devices
Related coursework: *Microelectronic Fabrication, IC Fabrication Lab, and Semiconductor Device Modeling*
CGPA: 3.76/4.00

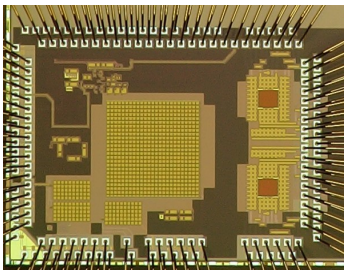
Indraprastha Institute of Information Technology (IIIT)-Delhi **August 2013 - June 2015**
Master of Technology

Advisor: Prof. M. S. Hashmi and Prof. Anuj Grover
Thesis: Identification of Weak Bits in SRAMs
Related coursework: *Memory Design and Test, Analog Circuit Design, Analog and Mixed Signal Design, Probability and Random Process*
CGPA: 8.30/10.00

JNTU Kakinada - Andhra Pradesh **September 2008 - April 2012**
Bachelor of Technology

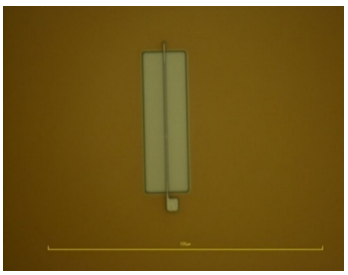
Advisor: Prof. P. Krishna Rao and Prof. S. Sridhrar
Related coursework: *Integrated circuits, Electronic Devices and Circuits, Network Topology, Digital Circuits, Microprocessors, Circuit Analysis, Probability and Stochastic Process (basic)*
Percentage: 81.68/100.00

E-Textile Battery-Less Walking Step Counting System with 23 pW Power on a Smart T-Shirt



An e-textile walking step counting full system integrated on a smart T-shirt is implemented. Harvesting from co-designed low-voltage triboelectric nanogenerator (TENG) pushes over-voltage protection/rectification on chip. Conformability and minimal off-chip components are achieved via dual-function harvester/sensor reuse and battery/passive elimination. Always-on power reduction to pWs enables uninterrupted operation while solely powered by breathing harvesting, suppressing the need for energy storage altogether. The level of integration is the highest for true system conformability and low cost for embedment into textiles.

FABRICATION PROJECT



In this project, a total of sixteen wafers—comprising eight p-type and eight n-type—were processed with various splits. To facilitate in-process monitoring, five additional test wafers were included to support measurement throughout the fabrication flow. Key fabrication steps such as photolithography, inductively coupled plasma (ICP) etching, standard cleaning, sputtering, and diffusion were meticulously executed to realize both NMOS and PMOS devices. Beyond the active devices, passive structures including gated diodes and cross-bridge configurations were also successfully fabricated. All fabricated active and passive devices underwent comprehensive evaluation using a four-probe station, confirming their successful operation.

OPEN SOURCE CIRCUIT DESIGN

Systematic Developement of Beta-Multiplier Circuit *March 2025 - Present*

- Characterized various flavors of core NMOS and PMOS devices using the Google SkyWater130 open-source PDK.
- Automated extraction of key device parameters—for NMOS and PMOS transistors.Source files and detailed instructions are available at ***skywater130nm PDK GMID***
- Developed systematic framework for designing conventional fixed transconductance circuit
- Preliminary results and detailed analysis are available at: ***anilkumargundu.github.io/resources***

Analysis and Design of Novel Fixed Trans-Conductance Circuit *March 2025 - Present*

- Proposed a novel approach for achieving fixed transconductance (gm) using a nested feedback loop architecture.
- Demonstrated improved PVT robustness in circuit-level simulations; layout implementation is in progress.
- Achieved enhanced loop stability through nested feedback and source regeneration techniques.

TECHNICAL SKILLS

Analog circuit design, Circuit analysis, Static Random Access Memories (SRAMs), SRAM memory characterization, Low power VLSI design, Static timing analysis (STA), Statistical analysis, and Flash memories.

LABORATORY EQUIPMENTS

Digital oscilloscope - Tektronix DPO71245, Teledyne Lecroy HDO6054 scope, Keithley source measure unit - 2636B (minimum spec: 0.1fA and 100nV), Keysight 2902B, 2902A, Agilent 2.5 GHz active probe, Power supply unit, Waveform generator, Digital multimeter, Capacitance measurement, Adaptive filter and buffer with Faraday's cage, National Instruments PXIe modular analog and digital system, Arduino boards - nano, atmega, and other versions, soldering station.

TOOLS & SIMULATORS

Circuit Simulators:
CADENCE SUIT for schematic simulations and layout, HSPICE, MEDICI, ELDO (SPICE), NGSPICE, MAGIC (LAYOUT), LTSPICE, ATLAS, SILVACO, MATLAB, WINSPICE
Device Simulators:
2D: ATLAS, SILVACO, MEDICI
3D: ATLAS 3D, ATHENE, Victory process, Mask View, Clever, Mixedmode, Devedit from SILVACO

CUTTING EDGE COURSES

Integrated Circuit Fabrication.
Microelectronics Device Modelling.
Nano system Fabrication (Lab Component).

SELECTED ACADEMIC PROJECTS

Fabrication of 0.5um n(p)-MOS Devices in Bulk-CMOS Technology *Feb 2018 - Apr 2018*

- Work done at Nano-system Fabrication Facility (NFF), HKUST.
- Sixteen wafers accompanied with five test wafers were processed in this project. Each wafer is divided into number of die's containing six NMOS and PMOS devices with various dimensions.
- Passive devices are also fabricated on the same die.

Statistical Analysis of Sense Amplifier for SRAMs Applications *May 2015 – July 2015*

- In this project, a latch type sense amplifier is designed and statistically analyzed the sense amplifier in terms of offset voltage and sensing delay.
- Random variations were introduced through Monte Carlo Method.
- Effects of sizing on offset voltage and sensing delay also tabulated.

Analysis of 6T, 5T, and 4T SRAM Cell w.r.t Various Design Metrics *May 2014 – July 2014*

- Analyzed 6T, 5T, and 4T SRAM cells w.r.t read and write operations.
- Compared their SNMs, write times, cell currents, and area.
- Circuit simulations are performed using ELDO and cadence.

Design of Memristor Emulator *Jan 2014 – Apr 2014*

- Designed an emulator circuit that behave like a memristor.
- Theoretically and experimentally verified the fingerprints of the memristor emulator in laboratory.
- Characteristics are compared for various operating frequencies.

PUBLICATIONS

Patent:

- **G. Anil Kumar**, L.Fassio, and M.Alioto, "Battery-less and inductor-less silicon chip architecture supporting dual-function motion harvesting and sensing for in-textile walking step counting", **SG Patent Application No. 10202401639T**(filed).

Journals:

- **G. Anil Kumar** and V. Kursun, "5nm Gate-All-Around Device Architecture with 3D Stacked Nano sheets", ***IEEE Transaction on Electron Devices*** (***TED***), February 2022 (in press).
- **G. Anil Kumar** and V. Kursun, "Novel Low Leakage and Energy Efficient Dual-Pullup/Dual-Pulldown Repeater," ***Integration, The VLSI Journal***. Vol. 78, Pp. 110-117, February 2021.
- **G. Anil Kumar** and V. Kursun "Low Leakage Clock Tree With Dual-Threshold-Voltage Split Input-Output Repeaters" , ***IEEE Transactions on Very Large Scale Integration*** (***VLSI***) ***Systems***, February 2019.
- **G. Anil Kumar** and V. Kursun, "Novel Gate-All-Around SRAM with Asymmetrical Counter-Doping", ***IEEE Transaction on Electron Devices*** (under manuscript revision for IEEE TED).

Conference:

- **G. Anil Kumar**, L. Fassio, M. Alioto, "E-Textile Battery-Less Walking Step Counting System with <23 pW Power, Dual-Function Harvesting from Breathing, and No High-Voltage CMOS Process, ***IEEE Symposium on VLSI Technology & Circuits***, June 2024 (accepted)
- **G. Anil Kumar** and V. Kursun, "Impact of Sheet Width and Silicon Height of 3D Stacked Nanosheet GAA Transistor Technology", (***IEEE International Symposium on Circuits and Sysytem***(***ISCAS***), June 2022)
- **G. Anil Kumar** and V. Kursun, "Optimization of 3D Stacked Nanosheet in 5nm Gate-All-Around Transistor Technology". ***33rd IEEE System-on-Chip Conference*** (***SOCC***). September 2021. (accepted for publication)
- **G. Anil Kumar** and V.Kursun "Energy Efficient Clock Distribution with Low-Leakage Multi-Vt Buffers" , 29th IEEE PATMOS, June 2019.
- **G. Anil Kumar**, M.S Hashmi, and Ramkesh Sharma "A Regression based Methodology for estimating SNM to Improve Yield of SRAM" , ***59th IEEE Midwest symposium on Circuits and Systems*** (***MWSCAS***), October 2016..
- N. Batra, S. Kaushik, **G. Anil Kumar**, A. Grover, M. S. Hashmi, and G. S. Visweswaran, " A Method to Estimate Effectiveness of Weak Bit Test: Comparison of Weak pMOS and WL Boost Based Test-28nm FDSOI Implementation," ***IEEE 29th International Conference on System on Chip*** (***SoCC***), September 2016
- N. Batra, **G. Anil Kumar**, A. Grover, M. S. Hashmi, and G. S. Visweswaran, "An Effective Test Methodology Enabling Detection of Weak bits in SRAMs: Case Study in 28nm FDSOI," ***IEEE 20th International Conference on VLSI Design and Test*** (***VDAT***), IIT Guwahati, India, May 2016.
- **G. Anil Kumar**, M.S. Hashmi, Anuj Grover, "A Modified Latch type Sense Amplifier with Improved Offset Voltage and Sensing Delay for High Speed SRAMs",***29th IEEE VLSI Design*** (***VLSID***) ***Conference***, Jan 2016, India.
- **G. Anil Kumar**, M.S. Hashmi, R. Sharma, N. Ansari, "Statistical Analysis and Parametric Yield Estimation of 6T SRAM Cell in Read Cycle w.r.t SNM for different capacities of SRAM".***28th IEEE System on Chip Conference*** (***SoCC***),September 2015, China.
- P. Sharma, **G. Anil Kumar**, and M. S. Hashmi, "Modeling and Yield Optimization of SRAM Sub-System for Different Capacities Subjected to Parametric Variations," ***IEEE 20th International Conference on VLSI Design and Test*** (***VDAT***), IIT Guwahati, India, May 2016.
- Rohan Sinha, M.S. Hashmi, **G. Anil Kumar** "A Novel Positive Level Shifter for High Speed Interfaces in Flash Memories ", ***18th IEEE VLSI Design and Test*** (***VDAT***), June 2014.
- Disha Arora, **G. Anil Kumar**, M.S.Hashmi," A High Speed Low Voltage Latch Type Sense Amplifier for Non-Volatile Memory", ***IEEE 20th International Conference on VLSI Design and Test*** (***VDAT***), IIT Guwahati, India, May 2016.
- Wazir Singh, **G. Anil Kumar**, "Design of 6T, 5T, and 4T SRAM Cell on Various Design Parametric", ***IEEE 9thINDIAcom***, December 2015, Delhi.

- **G. Anil Kumar**, W. Singh and S. M. Divi, "A proposed low-offset sense amplifier for SRAM applications," ***2nd IEEE Conference on Signal Processing and Integrated Networks*** (***SPIN***), March 2015, Noida.
- **G. Anil Kumar**, A. Srinivasan, M. S. Hashmi, "Comprehensive Analysis of 6T SRAM in FDSOI technology for Enhancing Yield" (technical report).

ACCOMPLISHMENTS

- Awarded with a medal for best performance in academics (2011-2012) by ministry of Andhra Pradesh.
- Research travel grant (RTG) from HKUST to attend SOCC 2021.
- VDAT 2015 IEEE conference fellowship recipient.
- VDAT 2015 IEEE Student fellowship recipient(IIIT-D).
- GATE scholarship for 2013 – 2014 academic year.
- Rank 99 in IIIT Hyderabad (entrance).

TEACHING EXPERIENCE

Teaching Assistant for CMOS VLSI Design	Sept 2020 – Dec 2020
Teaching Assistant for CMOS VLSI Design	Sept 2019 – Dec 2019
Teaching Assistant for CMOS VLSI Design	Sept 2018 – Dec 2018
Teaching Assistant for CMOS VLSI Design	Sept 2017 – Dec 2017
Course administrator for Basic Electronics	Aug 2016 – Dec 2016
Course administrator for Basic Electronics	Jan 2016 – Apr 2016
Students' project guide and grader for Analog Circuit Design	Aug 2015 – Nov 2015
Course administrator for Digital Circuits	Aug 2015 – Nov 2015
Teaching Assistant for Fields and Waves	Jan 2014 – Apr 2014
Teaching Assistant for Maths-3	Aug 2013 – Nov 2013

VOLUNTARY ACTIVITIES

- **Electroholics Club at IIIT-Delhi, India:**
  Organized and delivered a tutorial on basic analog circuits realized with combination of resistors, capacitors, inductors, and switches.
- **SPICE tutorial:**
  Organized a 3-day tutorial on Spice-Circuit simulator at IIIT-Delhi.

REFERENCES

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  Norwegian University of Science and Technology, Norway,
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- **Mohammad S Hashmi**

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